SECTION II. (AMENDMENTS TO THE CLAIMS)

A listing of claims 1-28 of the present application, which are amended herein with markings to show changes made, is provided below:

1. (Currently amended) A structure having an abrupt doping profile comprising:

a single crystal semiconductor substrate having an upper surface,

a first epitaxial layer of Ge over said upper surface,

said first epitaxial layer having a thickness ~~less than the critical thickness~~ in the range from about 0.5 nm to about 2 nm, said first epitaxial layer having a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant selected from the group consisting of phosphorus and arsenic, and

a second epitaxial layer of a semiconductor material over said first epitaxial layer.

2. (Original) The structure of claim 1 wherein said second layer comprises a material selected from the group consisting of Si and SiGe.

3. (Cancelled).

4. (Currently amended) The structure of claim 1 wherein said second layer has a concentration change of said dopant from said first layer into 40Å of said second layer of greater than 1×10^{19} atoms/cc.

5. (Original) The structure of claim 1 further including a third epitaxial layer of semiconductor material having a doping profile with a dopant concentration less than 5×10^{18} atoms/cc.

6. (Currently amended) The structure of claim 1 wherein said second epitaxial layer having a thickness of at least 300 Å and having a doping of [[P]] phosphorus less than 5×10^{16} atoms/cc for a predetermined thickness after its initial 300 Å thickness.

7-17. (Cancelled).

18. (Withdrawn) A method for forming abrupt doping within a semiconductor layered structure comprising the steps of:

selectively amorphizing a first layer having a high Ge content greater than 0.5, and crystallizing said amorphized first layer by solid phase regrowth.

19. (Withdrawn) The method of claim 18 wherein said step of selectively amorphizing includes the step of ion implantation.

20. (Withdrawn) The method of claim 18 wherein said step of selectively amorphizing includes first forming second and third layers about said first layer, said second and third layers having a Ge content less than 0.5.

21. (Withdrawn) The method of claim 18 wherein said step selectively amorphizing includes the step of first forming said first layer having a Ge content greater than 0.5.

22. (Currently amended) A field effect transistor comprising:

a single crystal substrate having a source region and a drain region with a channel therebetween and a gate electrode above said channel to control charge [[is]] in said channel, and

a first layer of Ge from about 0.5 nm to about 2 nm in ~~less than the critical~~ thickness and doped with a dopant selected from the group consisting of phosphorus and arsenic at a dopant concentration of greater than 5×10^{19} atoms/cc, wherein said first layer of Ge is positioned below said channel and ~~extending~~ extends through said source and drain regions.

23. (Cancelled).

24. (Original) The field effect transistor of claim 22 wherein said channel is in a second epitaxial layer selected from the group consisting of Si and SiGe formed over said first layer.

25. (Currently amended) A field effect transistor comprising:

a single crystal substrate,

a first layer of Ge from about 0.5 nm to about 2 nm in ~~less than the critical~~ thickness and doped with a dopant selected from the group consisting of phosphorus and arsenic at a dopant concentration of greater than 5×10^{19} atoms/cc, wherein said first layer of Ge is formed on said substrate,

a second layer of undoped SiGe epitaxially formed on said first layer,

a third layer of strained undoped semiconductor material selected from the group consisting of Si and SiGe,

a source region and a drain region with a channel therebetween, and

a gate electrode above said channel to control charge in said channel.

26. (Cancelled).

27. (Currently amended) A field effect transistor comprising

a single crystal substrate,

an oxide layer formed on said substrate having an opening,

a gate dielectric and gate electrode formed in said opening over said substrate,

a source and drain region formed in said substrate aligned with respect to said gate electrode,

a dielectric sidewall spacer formed on either side of said gate electrode and above a portion of said source and drain regions,

a first layer of Ge from about 0.5 nm to about 2 nm in ~~less than the critical~~ thickness and doped with a dopant selected from the group consisting of phosphorus and arsenic selectively positioned over exposed portions of said source and drain regions,

a second layer of semiconductor material selected from the group consisting of Si and SiGe doped with a dopant selected from the group consisting of phosphorus and arsenic epitaxially formed over said first layer to form raised source and drain regions,

28. (Cancelled).